Remarks and Arguments

Reconsideration is respectfully requested.

Claims 1-3, 5-12 and 16-17 are pending in the present application before this amendment. By the present amendment, claims 1, 2, and 16 have been amended.. No new matter has been added.

Amended claims 1, 2, and 16 include features in which the interposer base is defined by an upper principal surface, a lower principal surface and a sidewall surface; and a top principal surface of the electronic element is in direct contact with the lower principal surface of the interposer base. Amendments to the drawings are made to give reference numerals to the claimed --upper principal surface--, --lower principal surface--, --top end--, --bottom end--, and --top principal surface--.

Additionally, amendments to the specification have been made to correspond to the amended drawings.

In the office action (page 3), the examiner rejects claims 1-3, 5-11 and 16 under 35 U.S.C. §103(a) as being unpatentable over U.S. Publication No. 2004/0070064 (Yamane et al) in view of U.S. Publication No. 2003/0038415 (Anderson et al).

The applicants respectfully traverse the rejection and submit the claims, as they now stand, are in condition for allowance over the cited references.

Amended claim 1 recites:

--an electronic element; and

an interposer including an interposer base to which the electronic element is joined, and a plurality of post electrodes connected to corresponding electrodes of the electronic element;

wherein the electronic element and the interposer base are made of silicon,

said interposer base being defined by an upper principal surface, a lower principal surface and a sidewall surface connecting said upper principal surface and said lower principal surface, said plurality of post electrodes extending between said upper principal surface and said lower principal surface of said interposer, each of said plurality of post electrodes having a top end exposed at said upper principal surface, each of said plurality of post electrodes having a bottom end exposed at said lower principal surface,

said electronic element having a top principal surface in direct contact with said lower principal surface of said interposer, said electronic element carrying said plurality of electrodes respectively in correspondence to said plurality of post electrodes, said

plurality of electrodes being exposed at said top principal surface of said electronic element and in contact with corresponding bottom ends of said plurality of post electrodes.--

The applicants sincerely thank the examiner for the telephonic interview conducted on September 15, 2009, during which the examiner reviewed the amended claim 1 (claim 2 and claim 16 are similarly amended). During the interview, the examiner indicated that the amendment, which clarifies in more detail the features of the interposer base directly in contact with the electronic element, does not appear to be taught by the cited references. However, the examiner indicated that further review and a further search were necessary before making any conclusion as to whether the claims are in condition for allowance.

The presently claimed invention includes an interposer base (e.g., FIG. 1 21A) and an electronic element (e.g., FIG. 1, semiconductor chip 11).

The examiner's attention is respectfully directed to FIGs. 1 and 2A of the present application. As claimed, --said interposer base [is] defined by an upper principal surface, a lower principal surface and a sidewall surface connecting said upper principal surface and said lower principal surface--. Accordingly, with reference to FIGs. 1 and 2A, an upper principal surface 1, a lower principal surface 2 and a sidewall surface 3 connecting the upper and lower principal surface define the interposer base 21A and thus are outer surfaces of the interposer base 21A.

As claimed, --said electronic element [has] a top principal surface in direct contact with said lower principal surface of said interposer--. For example, in the present disclosure, a joining method is used in which the joint area of the electronic element and the joint area of the interposer base have highly smooth surfaces, and are placed in a vacuum environment and pressed together (specification page 20, line 27 to page 21, line 8)

Thus, in the present invention, a top principal surface of the electronic element is directly joined to a lower principal surface of the interposer base 21A (without requiring the use of adhesive, bumps or an underfill resin for joining purposes), where the lower principal surface along with the upper principal surface and the sidewall surface define the interposer base.

In the office action (page 3), the examiner cites Yamane and points to the 2nd semiconductor chip 20 and the bottom portion of item 50/72, 74 or 50/72 plus 74 as disclosing the claimed surface of the electronic element and surface of the interposer base integrated with each other by being brought into direct contact with each other.

As described above, the applicants have further clarified the present invention by clearly reciting that the top principal surface of the electronic element is in direct contact with the lower principal surface of the interposer base, where the lower principal surface together with the upper principal surface and the sidewall surface define the interposer base.

In Yamane, a portion of the first encapsulating resin 50/72 is removed so that a heated 2nd semiconductor chip 20 with bump electrodes 23 can be formed in the opening (Yamane FIG. 20K). An opaque resin 74 is then formed to encapsulate the second semiconductor chip 20.

As such, contrary to the presently claimed invention, Yamane requires the use of underfill resin 74 to support the semiconductor chip, and the semiconductor chip is encapsulated by the second encapsulating resin 74. That is, the second semiconductor chip 20 of Yamane is within and surrounded by the encapsulating resin 74, and thus no surface of the second semiconductor chip 20 contacts a lower defining surface of the encapsulating resin (as claimed, the interposer base is defined by the lower principal surface, the upper principal surface and the sidewall surface connecting the upper and lower principal surfaces).

In contrast to Yamane, the lower principal surface 2 of the presently claimed invention, which is a surface that together with the upper principal surface and the sidewall surface defines the interposer base (see, e.g., FIGs. 1 and 2A), is directly contacting the top principal surface of the electronic element.

Because Yamane discloses an encapsulant 74 (which the examiner analogizes to the interposer base) completely surrounding the second semiconductor chip 20, and because the claimed invention requires that the lower principal surface be a surface which together with the upper principal surface and the sidewall surface connecting the upper and lower principal surfaces define the interposer base, Yamane's 2nd semiconductor chip 20 encapsulated by the encapsulating resin 74 cannot disclose the

claimed --electronic element having a top principal surface in direct contact with said lower principal surface of said interposer--.

Anderson does not remedy the deficiencies of Yamane. Therefore, the applicants respectfully submit that neither Yamane nor Anderson, individually or in combination, teach or suggest the present invention of claim 1.

Additionally, claim 1 recites:

--each of said plurality of post electrodes having a top end exposed at said upper principal surface, each of said plurality of post electrodes having a bottom end exposed at said lower principal surface--

and

--said plurality of electrodes being exposed at said top principal surface of said electronic element and in contact with corresponding bottom ends of said plurality of post electrodes--

Accordingly, in the present invention of claim 1, the post electrodes are both exposed at top and bottom ends at the upper and lower principal surfaces respectively, and are in contact with the electrodes of the electronic element.

The applicants respectfully submit that Yamane in combination with Anderson does not teach this feature of the present invention.

In the office action (page 3), the examiner cites Yamane items 18 and 23 as disclosing the claimed post electrodes. Yamane's metal interconnects 18 do not contact electrodes of the 2nd semiconductor chip and are therefore unlike the post electrodes of the present invention.

Item 23 of Yamane are disclosed as being **bump electrodes 23**. These bump electrodes 23 do **not** have top and bottom ends exposed at upper and lower principal surfaces, respectively, as required by claim 1 (as noted above, the upper and lower principal surface are connected by the sidewall surface and the interposer base is defined by these surfaces).

Accordingly, for at least this additional reason, the applicants respectfully submit that neither Yamane nor Anderson, individually or in combination, teach or suggest the present invention of claim 1.

Independent claims 2 and 16 have been amended to include limitations corresponding to those of claim 1. Accordingly, the applicants respectfully submit that these claims are also in condition for allowance.

Claims 3 and 5-12 each depend from either claim 1 or claim 2. Accordingly, the applicants respectfully submit that these claims are in condition for allowance at least by virtue of their dependency as well as the additional limitations recited therein.

In the office action (page 4), the examiner rejects claim 12 under 35 U.S.C. §103(a) as being unpatentable over Yamane in view of Anderson, and further in view of U.S. Publication No. 2004/0150104 (Terui). In the office action (page 4), the examiner rejects claim 17 under 35 U.S.C. §103(a) as being unpatentable over Yamane in view of Anderson, and further in view of U.S. Publication No. 2003/0185484 (Chakravorty et al).

Claim 12 and claim 17 depend from claim 1 or 2 and claim 16 respectively. "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, in light of the above discussion of claims 1-2 and 16, the applicant submits that claims 12 and 17 are also allowable at least by virtue of their dependency as well as the additional limitations recited by each of these claims.

For the reasons set forth above, the applicants respectfully submits that claims 1-3, 5-12 and 16-17 pending in this application are in condition for allowance over the cited references. Accordingly, the applicants respectfully requests reconsideration and withdrawal of the outstanding rejections and earnestly solicits an indication of allowable subject matter. This amendment is considered to be responsive to all points raised in the office action.

When issuance of a Notice of Allowance is proper in the next action, the examiner is authorized to cancel the withdrawn claims, for which the applicant reserves the right to file a divisional application. Should the examiner have any remaining

questions or concerns, the examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

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